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(54) Title of the Invention : A Memory System

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SPECIFICATION

1. Title of the Invention

A Memory System

2. What we claim is :

1. A memory system characterized by being equipped with a plurality of

storage device blocks having different operating times, an address decoder which receives a system address signal and detects the access to the above - mentioned storage device blocks, a counter circuit which sets an initial value corresponding to the access time in the corresponding storage device blocks by the output signal of this address decoder and carries out the counting operation by the specific pulse signal, and a timing control device which sets the write or read operating time with respect to the storage device blocks by the output signal of this counter circuit.

2. A memory system, in accordance with Claim 1, characterized in that the above - mentioned counter circuit is constituted with a shift register.

3. A memory system, in accordance with Claim 1 or Claim 2, characterized in that the above - mentioned timing control circuit forms a timing signal by which to take in the read output signal in a latch circuit, and an operation completion signal to be sent to a central processing unit.

3. Detailed Explanation of the Invention

[Technical Field]

The present invention relates to a memory system, and for example, it pertains to the technology which is useful for the timing control of a memory system constituted with a storage device block which uses a high speed storage device / devices, and a storage device block which uses a low speed storage device / devices.

[Conventional Technology]

For example, in a case in which one memory system is constituted with a plurality of storage device blocks having different operating times such as a high speed RAM (random access memory) and a low speed RAM or a ROM (read only memory), as the operating times are different between or among storage device blocks, there arise the following problems in timing control thereof. If the control of all the storage device blocks is done by one single timing, all of the storage device blocks are operated by the operating timing of the slowest memory device blocks. On the other hand, if timing generating circuits are separately provided for respective storage device blocks and thus one tries to make an access

thereto at respective appropriate timings, the timing control circuit becomes complicated, and thus there arises a problem in that the number of constituting components increases.

[Purpose of the Invention]

The purpose of the present invention is to provide a memory system which allows a plurality of storage device blocks having different operating times to be accessed at the respective optimum timings by means of a simple constitution.

The above- mentioned and other purposes and characteristics of the present invention will become obvious and clarified by the test of the specification thereof and the drawings thereof.

[Summary of the Invention]

Let us explain one representative invention briefly as follows, out of the inventions to be disclosed in this Application. That is to say, a system address signal is received the access to the storage device blocks with different operating times is detected, an initial value corresponding to the access time in the corresponding storage device block is set by this output

signal, and the write or read operating time with respect to the plurality of the storage device blocks is set by the output signal of this counter circuit which carries out the time measuring operation by a pre-determined pulse.

[Examples embodying the Invention]

Fig. 1 shows a block diagram of one examples embodying the invention. In the memory system of this examples embodying the invention, through not especially limited only thereto, an explanation is given as to a case in which use is made of 2 types of storage devices, that is to say, a high speed storage device 6 and a low speed storage device 7.

In this examples embodying the invention, a timing control circuit as will be described below is used to control the timings of the above- mentioned storage devices 6 and 7. That is to say, an access to either of the above-mentioned 2 types of the memory devices 6 and 7 is detected by an address decoder 1 which receives a system address signal from an address bus AB. This detection output m 1 or m 2 is used as a selection signal of a selector 4. This selector 4 selects a storage means 2 or 4

which holds an initial value T 1 or T 2, and supplies the initial value T 1 or T 2 to a shift register 5. The above- mentioned initial value T 1 or T 2 is loaded on this shift register 5 by a timing signal ϕ 1 formed by the above- mentioned address decoder 1. Though not especially limited to this. this shift register 5 is constituted with a 10 bit shift register. The output signals D 7 through D 10 of the 7th bit section to the 10th bit section of the shift register 5 are supplied to the timing detection circuit constituted with the next AND gate circuit G 1 through G 4.

That is to say, the signal D 7 of the 7th bit section is inverted by an inverter circuit IV 1, and is supplied to the input side of the AND gate circuit G 4 together with the signal D 8 of the 8th bit side. The output signal of this AND gate circuit G 4 is used as a strobe signal of a latch register 8 which receives the read output signal D_{out} of the storage device 6 or 7. The output signal m 1 of the above- mentioned address decoder 1 and the output D 8 of the 8th bit section of the shift register 5 are supplied to the input section of the AND gate circuit G 2. The output signal CS of the AND gate circuit G 2 is used as a chip selection signal of

the high speed storage device 6. The output signal m 2 of the above-mentioned address decoder 1 and the signal D 8 of the 8th bit section of the above- mentioned shift register 5 are supplied to the input side of the AND gate circuit G 3. The output signal CS 3 of this AND gate circuit G 3 is used as a chip selection signal of the low speed storage device 7. In addition, the signal D 9 of the 9th bit section of the shift register 5 is inverted by means of the inverter circuit IV 2, and is supplied to the input side of the AND gate circuit G 1 together with the signal D 10 of the 10th bit section thereof. The output signal of this AND gate circuit G 1 is used as an operation completion signal ACK which is given to a central processing unit (CPU) which is not shown in the drawing here.

On the other hand, with respect to the storage device side which is to be controlled by the above- mentioned timing control circuit, the data input D_{in} of each of the storage devices 6 and 7 and the data output D_{out} which is through the above- mentioned latch register 8 are provided to the data bus DB through a bi- directional buffer 9. In addition, an address signal from the address but AB is supplied to each of the storage devices 6 and

7. (Not shown in the drawing).

Next, we shall explain the operations of the memory system as disclosed in this examples embodying the invention by referring to Fig.2 and Fig. 3.

Fig. 2 shows a timing diagram for a case in which an access is made to the low speed storage device 7 (m 2). In this examples embodying the invention, though not specifically limited to this, 0111111100 is held as an initial value T 2 in the storage means 3. Therefore, if a system address signal for selecting the storage device 7 is supplied to the address decoder 1, the output signal thereof m 2 is formed, and the above-mentioned initial value T 2 is supplied to the shift register 5 through the selector 4. And in synchronization with a load signal ϕ 1 formed by the clock ϕ, and this output signal m 2, the above- mentioned initial value T 2 is taken in the shift register 5. Therefore, with the timing of the clock ϕ shown in Fig. 1, the signals D 7 and D 8 of the 7th and 8th bit sections both become 1, and the remaining signals D 9 and D 10 of the 9th and 10 bit sections become 0. In this manner, the initial value T 2 is shifted in

sequence to the right hand side by 1 bit according to the clock ϕ. By this shift operation, the signals D 9 and D 10 become 1 in sequence, each being delayed by one clock. In addition, when the 7th clock arrives, as 0 of the first bit side in the initial value T 2 is shifted to the 7th bit side, the signal D 7 becomes 0. Thereafter, the signals D 8 through D 10 are allowed to change to 0, each being delayed by one clock. In the above-mentioned shift operation of the shift register 5, the storage device 7 (M 2) is selected by the output signal CS 2 of the AND gate circuit G 3 which receives the above- mentioned signal D 8 of the 8th bit side, and the selection signal (logic "1") of the output signal m 2 of the above-mentioned address decoder 1. And because when the signal D 7 changes to 0 (low level), the strobe signal ϕ 2 is formed, the read signal D_{out} from the storage device 7 is taken in the latch register 8 if it is a read operation. Furthermore, since the signal D 9 becomes 0 with a delay of 2 clocks, the operation completion signal ACK is generated by the by the AND gate circuit G 1, and that access is terminated. That is to say, the central processing unit (CPU) (which is not shown in the drawing)

receives the above- mentioned operation completion signal ACK, and then receives the above- mentioned read data D_{out} through the bi-directional buffer. Furthermore, if it is a write operation, the input data D_{in} is supplied to the storage device 7 during the above- mentioned chip selection period CS 2, and the operation is allowed to be terminated by waiting the arrival of an operation completion signal ACK similar to the above.

Fig. 3 shows the timing diagram for a case in which an access is made to the high speed storage device 6 (M 1). In this examples embodying the invention, though not especially limited thereto, 0000011100 is held in the storage means 2 as the initial value T 1 thereof. Therefore, when a system address signal for the selection of the storage device 6 is supplied to the address decoder 1, the output signal thereof m 1 is formed, and the above- mentioned value T 1 is supplied to the address register 5 through the selector 4. And, in synchronization with the load signal ϕ 1 formed with the clock ϕ and the output signal m 1 thereof, the above- mentioned initial value T 1 is taken in the shift register 5. Therefore, with the

timing of the clock ϕ shown in Fig. 1, the signals D 7 and D 8 of the 7th and 8th bit sections become 1, and the signals D 9 and D 10 of the remaining 9th and 10th bit sections become 0. The initial value T 1 such as this is shifted to the right hand side in sequence by 1 bit according to the clock ϕ. By this shift operation. the signals D 9 and D 10 become 1 in sequence, each being delayed by 1 clock. In addition, when the 3rd clock ϕ arrives, 0 of the 5th bit section in the initial value T 1 is shifted to the 7th bit section and therefore the signal D 7 becomes 0. After this, D 8 through D 10 change to 0 in sequence, each being delayed by one clock.

By the above- mentioned shift operation of the shift register 5, the storage device 6 (M 1) is made to assume a selected state by the output signal CS 1 of the AND gate circuit G 3 which receives the above-mentioned signal D 8 of the 8th bit section and the selection signal (logic "1") of the output signal m 1 of the above- mentioned address decoder circuit 1. And when the signal D 7 changes to 0 (low level), a strobe signal ϕ 2 is formed, and therefore if it is a read operation, the read signal

D_{out} from the storage device 6 is taken in the latch register 8. In addition, since the signal D 9 becomes 0 with a delay of 2 clocks, the operation completion signal ACK is sent out by means of the AND gate circuit G 1, and the access thereto is ended. That is to say, a central processing unit (CPU) which is not shown in the drawing receives the above- mentioned operation completion signal ACK, and then receives the above- mentioned read - out data D_{out} through the bi- directional buffer. On the other hand if it is a write operation, the input data D_{in} is supplied to the storage device 6 during the above- mentioned chip selection period CS 1, and the operation is terminated by waiting for the transfer of the operation completion signal similar to the above-mentioned one.

By the above- mentioned operation, the low speed storage device 7 is made to assume an operating state during a period of 7 clock portions of the clock ϕ, while the high speed storage device 6 is made to assume an operating state during the 3 clock portions of the clock ϕ. Therefore, in this examples embodying the invention, the operating time of a memory

device is made to coincide by one cycle of the above- mentioned clock ϕ and the number of clocks. The setting of such an operating time (access time) can be simply and easily achieved by the setting of the above-mentioned initial values.

[Effects of the Invention]

(1) An effect is achieved to the effect that even if a memory system is constituted with a plurality of storage devices which have different operating times, it is possible to obtain a memory system which can be operated at a cycle / cycles corresponding to the operating time / times of the respective storage devices, by a single timing control circuit which is constituted with a simple constitution of an address decoder, a shift register, a selector, and gate circuits, etc.

(2) Since it is possible to control a timing by a simple circuit as mentioned in the above- mentioned Item (1), there is an effect to the effect that the failure rate of the whole system can be reduced.

(3) Since it is possible to reduce the number of the constituting components of the timing control circuit as mentioned in the above-

mentioned Item (1), an effect is achieved to the effect that it is possible to obtain a memory system of a lower cost.

(4) Since each of the storage devices can be accessed at the optimum operating cycle as mentioned in the above- mentioned Item (1), there is no waste in memory access time. Therefore, an effect is obtained in that storage information can be inputted or outputted in a reasonable manner.

In the above, we have explain the invention achieved by the inventors of the present invention in a specific and concrete manner based on the examples embodying the invention, and it is a matter of course that the present invention is not limited nor restricted only to the above-mentioned examples embodying the invention, and that the present invention can be worked in a various manner as long as the gist and tenor of the present invention is not deviated. For example, with respect to 3 types or more of storage devices, if storage means for holding the above-mentioned initial values and gate circuits are added, it is possible to control the timings corresponding to the respective operating times in the same manner as above. In addition, in a case in which time setting

corresponding to the operating times of the whole storage devices, it is also permissible to utilize a time measuring (pulse counting) circuit such as a programmable counter in place of the above- mentioned shift register.

In addition, the configuration of a specific circuit for each circuit block can assume various modes of implementation or working.

[Field of Utilization]

The present invention can be widely and broadly applied to a memory system comprising a plurality of storage devices having different operating times.

4. Simple Explanation of the Drawings

Fig. 1 shows a block diagram of one examples embodying the invention of the memory system in accordance with the present invention.

Fig. 2 shows a timing diagram by which to explain the timing control of a low speed storage device.

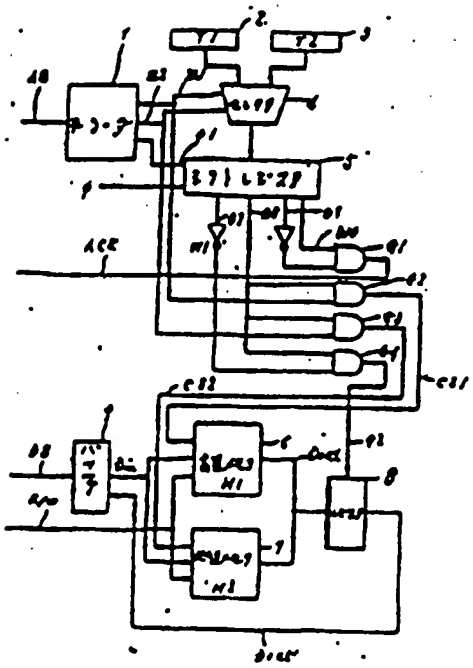
Fig. 3 shows a timing diagram by which to explain the timing control of a

high speed storage device.

1 is an address decoder, 2 and 3 are storage means, 4 is a selector, 5 is a shift register, 6 is a high speed storage device, 7 is a low speed storage device, 8 is a latch register and 9 is a bi- directional buffer.

Agent . Patent Agent, Akio Takahashi (seal impression)

Fig. 1



key 1 address decoder, 4 selector, 5 shift register, 6 high speed storage memory, 7 low speed storage memory, 8 latch register, 9 bi- directional buffer

Fig. 2

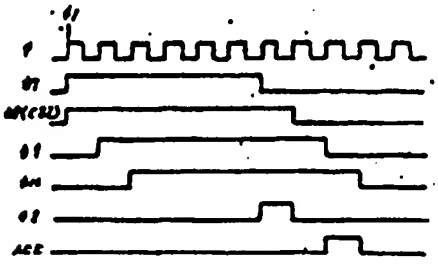


Fig. 3